What is claimed is:

1. A method of autocalibrating a plurality of phase-delayed clock signal edges within a reference clock period, comprising:

measuring delay spacings between said plurality of clock signal edges;

calculating desired delay spacings from said delay spacings;

calculating ideal signal edges from said desired delay spacings; and

adjusting said clock signal edges to match said respective ideal signal edges;

wherein said plurality of clock signal edges are selectively available.

2. The method of claim 1, further comprising:

measuring a wrap-around delay spacing between the last and first signal edges of said plurality of clock signal edges to reduce error in said calculation of desired delay spacing.

3. The method of claim 1, wherein said desired delay spacings are calculated by:

calculating an average delay spacing so that the calibrated clock signal edges form an approximately linear time reference.

4. The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edge, said delay spacings are measured by:

comparing the first and second clock signal edges to determine which arrives first.

5. The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

switching first and second clock signal edges of said plurality of clock signal edges to target and delay signal paths, respectively; and

comparing the phases of said first and second clock signal edges.

6. The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

delaying a first clock signal edge of said plurality of clock signal edges by one period with a one period delay circuit; and

comparing the phases of said first clock signal edge to the phase of a second clock signal edge of said plurality of clock signal edges.

7. The method of claim 1, wherein said delay spacings are measured by:

delaying a first clock signal edge of said plurality of clock signal edges to determine said delay spacing.

8. The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

adjusting a first clock signal to match a second clock signal edge, each of said first and second clock signals of said plurality of clock signal edges; and

determining said delay spacings from said adjustment.

9. The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

incrementing a calibration control register to induce a change in delay of a first clock edge to match a delay of a second clock edge, said first and second clock edges of said plurality of clock signal edges; and

taking the resulting value of the calibration control register as the delay spacing measurement.

10. The method of claim 1, wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by:

decrementing a calibration control register to induce a change in delay of a first clock edge to match a delay of a second clock edge, said first and second clock edges of said plurality of clock signal edges; and

taking the resulting value of the calibration control register as the delay spacing.

11. The method of claim 1, further comprising:

calculating error delays between said clock signal edges and respective next ideal signal edges to enable said adjusting of said clock signals based on said calculated error delays.

12. The method of claim 11, further comprising:

saving said error delays for subsequent retrieval.

13. An apparatus for measuring the time delay between adjacent clock edges, comprising:

target and delay signal paths;

a variable delay module in said delay signal path, said delay cell having a delay bias input; and

a phase detector having respective inputs coupled to said target and delay signal paths;

wherein said variable delay module is operable to delay a first clock signal on said delay path so that a bias input signal presented to said delay bias input, when a bias input signal is present, corresponds to the time delay between said first clock signal and a second clock signal on said target signal path.

14. An apparatus according to claim 13, wherein said variable delay module further comprises:

a single period delay circuit; and

a variable delay cell coupled to said single period delay circuit, said delay cell having said delay bias input and said bias input signal corresponding to a variable time delay between said first and second clock signals.

15. The apparatus according to claim 13, further comprising:

a biasing switch connected to select among different bias input signal levels for application to said delay bias input.

16. The apparatus according to claim 15, further comprising:

a variable voltage source which provides said different bias input signal levels;

17. The apparatus according to claim 16, wherein said variable voltage source comprises an impedance string coupled between first and second reference voltages with taps that establish a monotonic set of bias voltages between said first and second reference voltages.

18. The apparatus according to claim 17, wherein said biasing switch comprises a multiplexer (MUX) having a plurality of inputs from said taps and an output coupled to said delay bias input.

19. The apparatus according to claim 18, further comprising:

a plurality of calibration edge registers coupled to said MUX to store switch positions for said MUX.

20. The apparatus according to claim 13, wherein said phase detector further comprises:

an inverting input coupled to one of said target and delay signal paths;

a non-inverting input coupled to the other of said target and delay signal paths; and

a phase detector output;

the polarity of the signal at the detector output varying in accordance with whether a clock signal on the target path or the delay signal path reaches the detector first.

21. The apparatus according to claim 20, further comprising:

a multiplexer (MUX) having a plurality of clock inputs and an output;

a switch connected to selectively apply said MUX output to either said delay or target path.

22. The apparatus according to claim 21, further comprising:

a multi-phase clock generator having a plurality of clock timing outputs, each timing output coupled to a re-

spective MUX clock input so that said multi-phase clock generator is operable to cooperate with said MUX to selectively introduce said clock edges to said switch for application to said target and delay signal paths.

23. A method of calibrating a timing vernier, comprising:

autocalibrating a plurality phase-delayed clock signal edges to match respective ideal signal edges, said phase-delayed clock signal edges dividing one period of a reference clock;

comparing a vernier clock signal edge to one of said plurality of phase-delayed clock signal edges after said phase-delayed clock signal edges have been autocalibrated;

adjusting said vernier clock signal edge to match said one phase-delayed clock signal edge;

wherein said clock edge is calibrated and available for calibrated use by a user.

24. The method of claim 23, wherein said autocalibrating comprises:

calculating an average measurement delay between said phase-delayed clock signal edges to determine said ideal signal edges; and

adjusting said plurality of phase-delayed clock edges to match said ideal signal edges.

25. An apparatus for measuring the time delay between adjacent phase-delayed clock edges, comprising:

a plurality of clock signal lines;

means for comparing first and second clock signal edges, when said first and second clock signals are pre-

sent, said means for comparing connected to said phase-shifted clock signal lines;

means for measuring delay spacing between said first and second clock signals, when said clock signals are present; and

means for selectively adjusting said first clock signal to match said second clock signal, when said first and second clock signals are present;

wherein said means for measuring is operable to capture measurement delay spacing between said first and second clock signals after said means for adjusting has adjusted said first and second signals to match each other.